iNEMI TIN WHISKER PROJECTS: TEST DEVELOPMENT, RISK MITIGATION, AND FUNDAMENTAL THEORY DEVELOPMENT

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Abstract: Since 2001, the International Electronics Manufacturing Initiative (iNEMI) has had three very active - and successful - projects addressing various aspects of having electroplated lead-free, tin-based surface finishes in the electronics supply chain. The iNEMI Tin Whisker Accelerated Test Project identified tests to promote whisker formation, the iNEMI Tin Whisker User Group developed guidelines for minimizing risk of failure from tin whiskers in consumer and high-reliability electronic applications, and the iNEMI Tin Whisker Modeling Project focused on identifying the root causes of whiskers. All three projects made significant contributions to the electronics industry's understanding of tin whiskers as a potential failure mechanism and to tools and standards necessary for controlling processing factors to reduce the likelihood of tin whiskers.

The three original tin whisker projects have been completed and, in 2007, iNEMI organized the iNEMI Analytical Tin Whisker Test Group. This latest project combines teams from, and extends the results of the Modeling and Accelerated Test projects. This latest effort is continuing to develop predictive tests that will accelerate whisker growth, using theories formulated by the previous projects to explain the formation of tin whiskers. The results from the four iNEMI projects will be discussed as well as the implications with respect to risk mitigation.

1. INTRODUCTION

In 1956, Arnold [1] determined that small additions of Pb (3-10%) to electrodeposited Sn surface finishes eliminated the spontaneous formation of Sn whiskers on electronic components. The suppression of tin whisker formation lowered the risk of premature failure in electronics due to short circuits formed by tin whiskers bridging between adjacent leads and to plasma formation in low pressure environments, i.e. aerospace applications. The use of low levels of Pb in Sn-based surface finishes, therefore, became standard practice for consumer and high-reliability electronic systems for over fifty years. When the Pb is removed from the plating the propensity for whiskering increases. A typical example of tin whiskers forming spontaneously on a matte tin plated SOIC after 3 years of ambient storage is seen in Figure 1.

With the European Union (EU) ban of even small amounts of Pb in surface finishes in electronic components slated to start in July 2006, major companies within the electronics industry worldwide began to study the current state-of-the-art of Pb-free tin electroplating with respect to whisker formation. [3,14,17] In 2001 there were no standard test methods for determining the tendency of a component finish, a plated component lead, or an assembly to form whiskers. A number of studies on accelerated methods and on ambient whisker formation and growth had been completed with in many cases conflicting results.

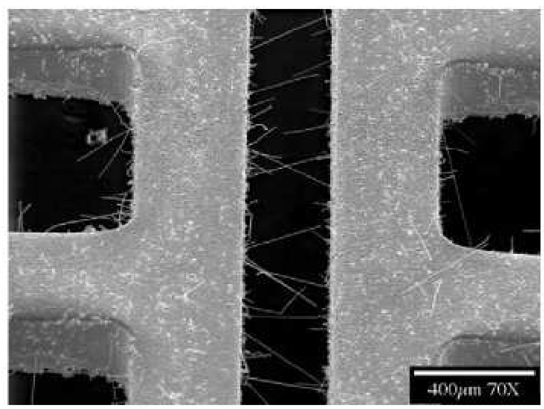


Figure 1 Matte-tin plated SOIC after 3 years of ambient storage.

Beginning in 2001 International Electronics Manufacturing Initiative (iNEMI) member companies focused through three major iNEMI projects on (1) developing robust test methods for assessing the propensity of Sn and Pb-free Sn alloy films to form tin whiskers (iNEMI Tin Whisker Accelerated Test Group), (2) developing a set of mitigation practices that, if applied, would lower the probability of tin whisker formation (iNEMI Tin Whiskers User Group), and (3) understanding the root causes of tin whisker formation with the end goal of using this fundamental understanding to design predictive test methods and mitigation strategies that would be as effective as Pb in stopping whisker formation (iNEMI Tin Whisker Fundamentals and Modeling Group). As described in detail by Reynolds, Lee, and Smetana [14], the iNEMI Tin Whisker Accelerated Test Methods Group was the first iNEMI project team to form. It quickly became clear to the Group that the standard accelerated test conditions traditionally used for components and printed wiring board assemblies, such as exposure to higher temperatures, humilities and thermal cycling ranges than devices are typically exposed to when in field use, were not going to lead in the short term to a single, simple test for predicting tin whisker formation, and therefore for qualification specifications. The team developed a three-front approach to fulfilling both short term needs created by Restriction of Hazardous Substances Directive (RoHS) and Waste Electrical and Electronic Equipment Directive (WEEE) legislation and longer term needs for reducing the risk of tin whisker-induced failure. According to Reynolds, Lee, and Smetana [14], the steps defined by the iNEMI Group members were: (1) to define a set of test conditions to induce whisker growth, identify the relevant whisker parameters that categorize whisker growth, and recommend a protocol for measuring and recording the whisker formation data; (2) to develop "acceptance test criteria and mitigation practices that would provide an interim auxiliary tool to minimize reliability exposures of long-life reliability sensitive electronic systems; and (3) to develop a fundamental understanding of tin whisker formation that could be used to improve upon (1) and (2). These three steps translated into the iNEMI Tin Whisker Accelerated Test Group, the iNEMI Tin Whisker User Group, and the iNEMI Tin Whiskers Fundamentals and Modeling Group, respectively. In 2008, the three groups reorganized to form the iNEMI Analytical Tin Whisker Test Group to address the lack of understanding about the mechanisms for tin whisker formation and of the relationship between test conditions and use conditions.

The goals and some of the most significant results of the four iNEMI tin whisker projects are presented in the context of the state-of-the-art in tin whisker understanding and mitigation as of 2010.

2. iNEMI TIN WHISKER ACCELERATED TEST GROUP

The iNEMI Tin Whisker Accelerated Test Group developed and conducted five individual studies that revealed some of the intrinsic variability in what factors and interactions affect tin whisker formation and tin whisker-induced failure. Highlights from the Phase 1-3 studies are described below; more detailed analysis is provided in [11, 14, 16, 21]. The results of Phase 1-3 studies served as the foundation for JEDEC standards JESD22A121, "Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes" [9] and JESD201 "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes" [8]. With the completion of the Phase 3 study, the iNEMI Tin Whisker Accelerated Test Group turned its attention to the effects of environment on the propensity for whisker growth. A design-of-experiments (DOE) study, DOE 4, examined the effects of bias and current flow on tin whisker formation and to evaluate tin whisker formation on soldered assemblies. The fifth study DOE 5 was directed at determining if a single acceleration function could be empirically found that could define a mathematical relationship between whisker propensity and environmental conditions (temperature and humidity).

2.1 Phase 1

In Phase 1, brass coupons and eight-lead small-outline integrated circuit (SOICs) were electroplated in a research laboratory with either bright tin from a single supplier or SnPb. The plated samples were exposed to one of two preconditioning methods, followed by five storage environments with a maximum exposure time of four weeks. Under these conditions, whiskers formed only on the brass coupons and at much lower levels than expected. The group postulated that (1) the absence of whiskers from a bright film that was expected to form whiskers may have been due to lower levels of impurities or contamination in laboratory plating conditions than in commercially plated samples, (2) the surface finishes on the SOIC terminations had been cracked during lead formation and, therefore, the compressive stresses in the surface finishes were relaxed compared with uncracked films, and (3) the exposure times were too short to promote whisker growth. While the results were inconclusive, they served as the basis for the plan for Phase 2.

2.2 Phase 2

In Phase 2 eight-lead SOIC packages were matte-tin plated with thin and thick platings using methane sulfonic acid (MSA)-based and sulfate-based electrolytes by two different suppliers. The test conditions included ambient (30°C for 5 months), two temperature and humidity combinations (30°C/90%RH and 60C/95%RH), thermal cycling (-55°C to 85°C, with 20 minute cycles and 7 minute dwell times), and a combination of all the above conditions. In addition to the matte Sn-plated SOIC samples, thin bright Sn surface finishes on brass coupons and thick 90Sn/10Pb surface finishes on SOIC samples were used as controls. The test conditions were also examined for an additional sample cell of passive components (fuses) that were barrel plated with a Ni barrier layer and a pure Sn layer. In terms of test conditions, thermal cycling generally produced higher whisker densities than the other test conditions, with the maximum whisker length increasing with whisker density. Subsequent temperature or humidity exposure following thermal cycling did not significantly increase either whisker density of length. The bath chemistry/plating process and the plating thickness had significant effects on tin whisker growth. There were multiple interactions between variables that led the Group to focus on defining the acceptance test conditions using three proposed test conditions with longer durations, with production plated 64lead quad flat pack components (QFP) using a wider range of surface finishes and comparison cells, including matte Ni underplating, melted or

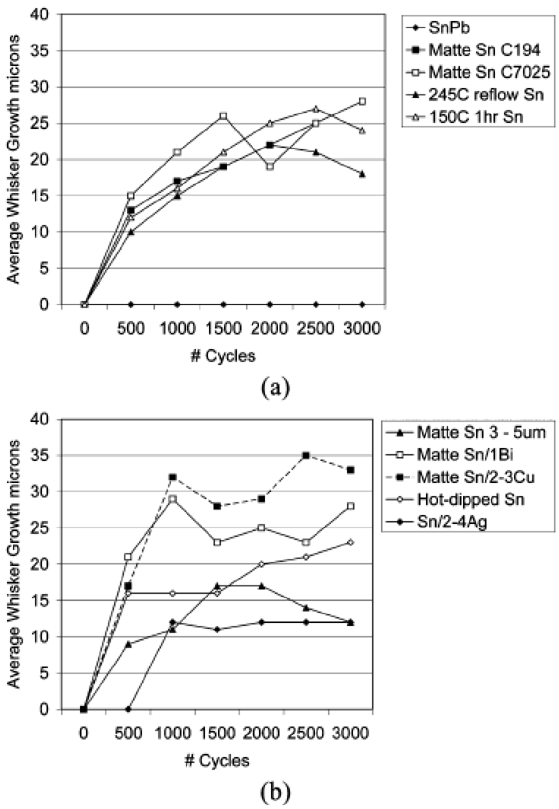


Figure 2. Whisker growth over time for various surface finishes exposed to thermal cycling conditions of -55°C to +85°C (air to air, 20 minute cycles). (Figure taken from [16].)

annealed Sn, hot-dipped Sn, and the JEITA test vehicle.

2.3 Phase 3

The detailed description of the iNEMI Phase 3 experimental plan, results, and analysis for the fifteen different sample types, including tin and tin alloy compositions, can be found in Reynolds, Lee, and Smetana, with the main results and their integration into JESD22A121 summarized [13]. Of special note from Phase 3 is the test plan required repeated scanning electron microscope inspection for tin whiskers at the following intervals: (1) for thermal cycling at -55°C to +85°C (air to air, 20 minute cycles), inspections were performed at 500 cycle intervals for a total duration of 3000 cycles; (2) 60°C/93%RH at either 1000h or 2000h intervals up to 9000h; and (3) ambient conditions (20°C-25°C with 20%-60%RH) at 1000h-3000h depending on sample type with a maximum duration of 10000h. The results of Phase 3 demonstrated that short-term testing results could not be used to provide a relative ranking for surface finishes, or to evaluate quality control for the ostensibly the same plating conditions. The results from Phase 3 were used (1) to set lower humidity conditions and require better chamber control to prevent condensation in the high temperature/high humidity condition, (2) to set 96 leads as the minimum number of inspected leads for a valid test, (3) to require humidity control (60%RH) for ambient testing, and (4) to validate the JEDEC test intervals and durations for the ambient and high temperature/humidity conditions (1000h for a 4000h total duration), and thermal cycling conditions (500 cycles for a total duration of 1500 cycles.) The latter can be seen for Phase 3 thermal cycling results in Figure 2, where the total duration of 1500 cycles provides sufficient differentiation for the sample combinations examined..

2.4 DOE 4

In 2004-2005, DOE 4 was designed and carried out to evaluate the formation of whiskers on soldered assemblies and the effect, if any, of electrical bias and/or current flow on tin whisker growth. Three different component package types encompassing seven different base material, lead finish combinations were tested with 4 different test variables; voltage (3 levels), current (2 levels), temperature and humidity conditions (2 levels), and solder paste (2 levels), as shown in Figure 3. Given the effects of multiple factors and their interactions on tin whisker formation, DOE 4 illustrates the number of variables that are required to examine any effect with any certainty. The experimental challenges in DOE 4 exemplify the difficulty with performing tin whisker research with adequate control over all the variables.

Fig. 4 shows a simplified schematic diagram of how the different voltage and current variables were achieved on the design. This simplified schematic is representative of how this was done on the 2 QFP packages. For the SOIC packages, 3 different devices were used to achieve the various combinations. Fig. 5 shows one of the actual assembly sub-boards designed for simplified removal from the base printed circuit board to allow them to fit in an SEM for inspection and to reduce damage to whiskers that may have formed during the test exposures.

Assembly was done using SnPb and SAC solder pastes according to the test matrix (Figure 3) using standard assembly processes and reflow profiles suitable for each alloy. The solder paste wetting of the leads of the devices was extensive. For the 64 lead

DOE : Effect of Bias on Whisker Growth

Constants:

Experimental units:

Part Type	Description
32 LQFP	Matte Tin on 7025
32 LQFP	Bright Tin on 7025
32 LQFP	Tin-Lead on 7025
64 LQFP	Matte Tin on 194
64 LQFP	1µm Semi-Bright on 194
16 SOIC	Matte Tin on 194
16 SOIC	Matte Tin on 7025

Plating Thickness: 10 microns except where noted

Variables:	**Levels:**
A: Voltage	high: 40V low: 5V 0V
B: Current*	high: 500uA low: 0
C. Temp/Humid	high: 60C/93RH low: ambient
D: Finish	high: bright tin (<1um, measure grain sz, stress, orientation, save waste from lf) low: matte tin (>1um, measure grain sz, stress, orientation, save waste from lf) SnPb
E: Basis Metal	high: Olin 194 low: C7025
F: Solder Paste	high: Sn/37Pb low: Sn/3.8Ag/0.7Cu

Read points:

0; 1500hrs; 3000hrs

Run	Finish	Basis Metal	Solder Paste	40V				5V				0	
				500uA		0		500uA		0		0	
				Amb	60C/93RH	Amb	60C/93RH	Amb	60C/93RH	Amb	60C/93RH	Amb	60C/93RH
1	bright tin	C7025	SnPb	2	2	2	2	2	2	2	2	2	2
2	bright tin	C7025	SnAgCu	2	2	2	2	2	2	2	2	2	2
3	matte tin	C7025	SnPb	2	2	2	2	2	2	2	2	2	2
4	matte tin	C7025	SnAgCu	2	2	2	2	2	2	2	2	2	2
5	matte tin	Olin 194	SnPb	2	2	2	2	2	2	2	2	2	2
6	matte tin	Olin 194	SnAgCu	2	2	2	2	2	2	2	2	2	2
7	SnPb	C7025	SnPb	2	2	2	2	2	2	2	2	2	2
8	1um bright tin	Olin 194	SnPb	2	2	2	2	2	2	2	2	2	2
9	2nd matte tin	C7025	SnPb	2	2	2	2	2	2	2	2	2	2
10	2nd matte tin	Olin 194	SnPb	2	2	2	2	2	2	2	2	2	2

Figure 3

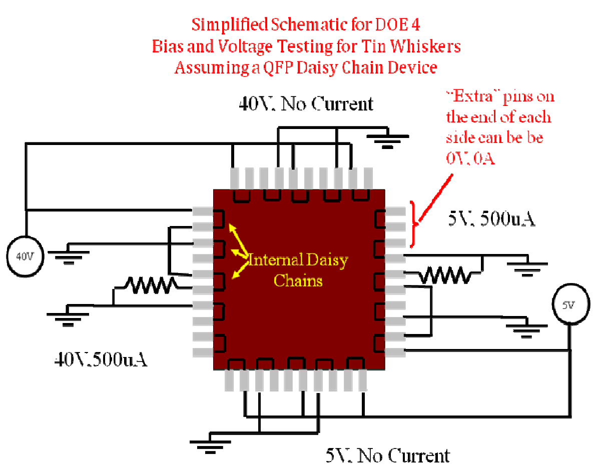


Figure 4: Simplified schematic of the test setup used to achieve the different voltage and current options.

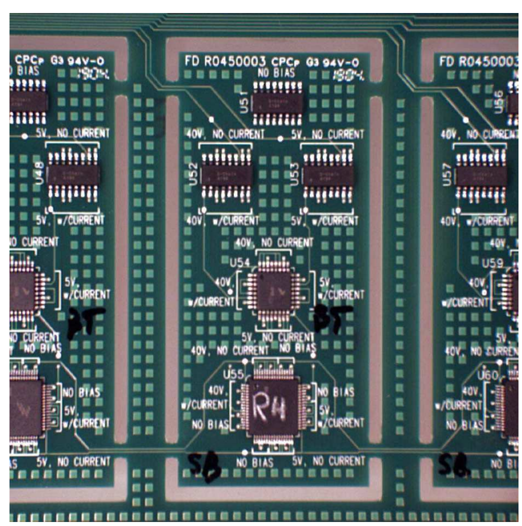


Figure 5: Test board assembly for DOE 4

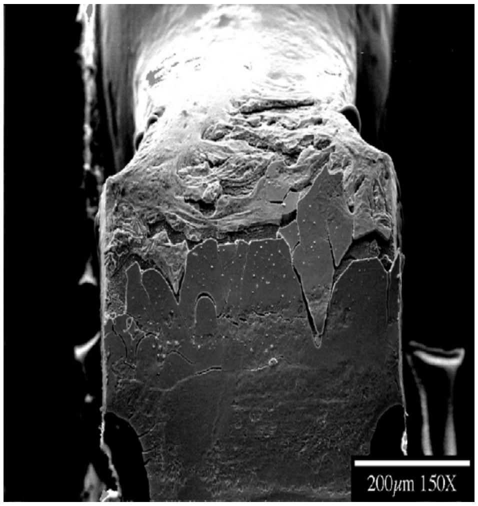


Figure 6: 32LQFP, bright Sn, Sn/Ag/Cu solder. All leads exhibited gross cracking and/or irregular reflow.

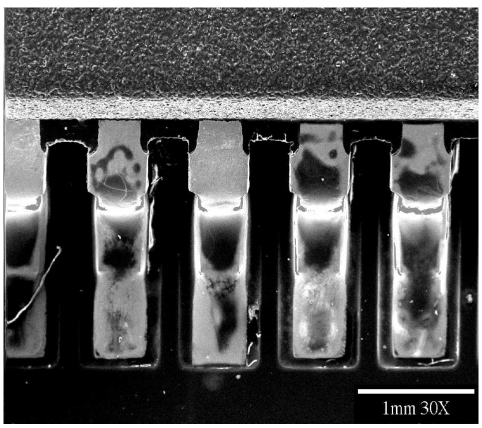


Figure 7: 32 LQFP, matte Sn. Flux residue

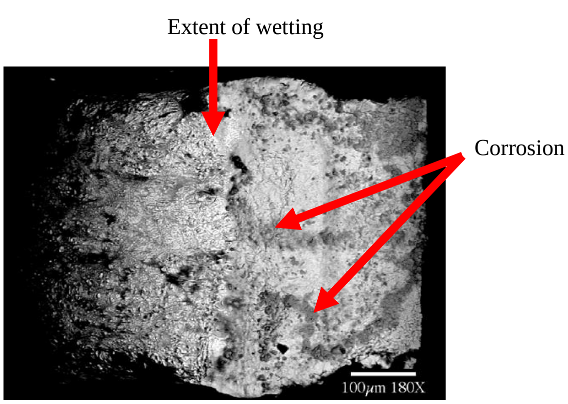


Figure 8: 16 SOIC, matte Sn, Sn/Pb solder, after 1500 hours of 60°C/86%RH

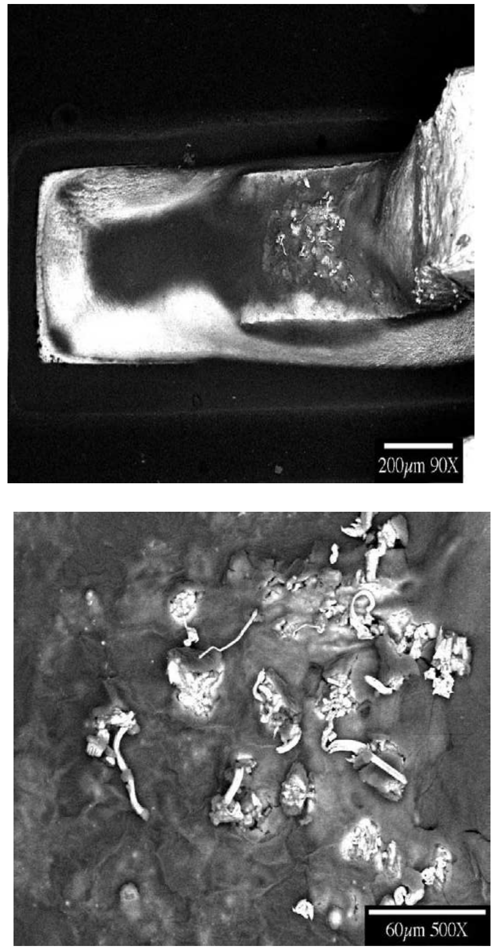


Figure 9. 32- LQFP, bright Sn finish, Sn/Ag/Cu solder, Example of leads with whiskers growing on the foot area where alloyed with the solder. Top picture shows the area, Bottom is a close-up.

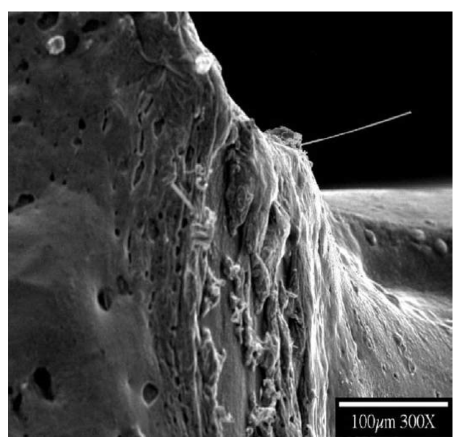


Figure 10. Example of a long whisker on 32 LQFP, bright Sn finish, Sn/Ag/Cu solder

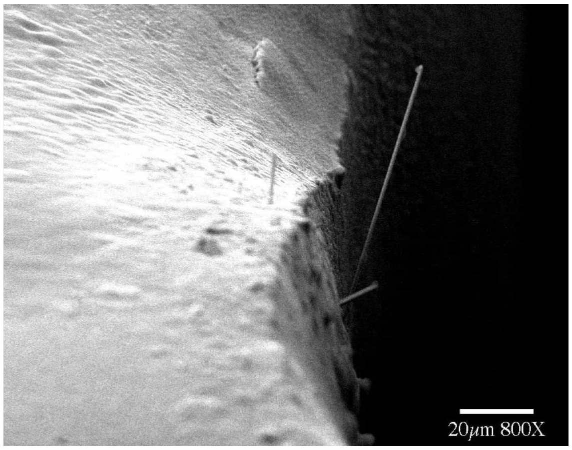


Figure 11: 32LQFP, matte Sn finish, Sn/Ag/Cu solder. Example of whiskers

Low-profile Quad Flat Package (64 LQFP) devices with the matte tin finish, 100% of the lead surfaces were fully wetted with solder regardless of which solder paste was used. The semi-bright tin finish on this device wetted to approximately the shoulder of the lead. For the SOIC and the 32 LQFP devices, wetting typically extended to the shoulder of the leads. The bright tin plating used on these devices was found to be incompatible with reflow resulting in gross cracking and/or irregular reflow, as seen in Figure 6. Because of the extensive wetting of the surfaces with solder, there was very little remaining "unalloyed" lead finish, and ultimately the testing would be testing primarily alloyed finishes with the assembly solders. Considering this result, it would have been better to use a non-standard soldering process with less solder paste to reduce the wetted areas on these components. Flux residue was common on the assembled parts as typical for soldered assemblies, as seen in Figure 7. No whiskers were seen in the ambient storage condition for any sample. After 1500 hours of 60°C/85% relative humidity, whiskers were found on only 3 leads, none of which had any bias or current. Two of these whiskers, both under 50μm in length, were on the semi-bright tin on the 64LQFP solder with SnPb solder. Short whiskers were found on a 32LQFP, matte Sn finish soldered with Sn/Ag/Cu solder in an area adjacent to corrosion on the matte tin. Corrosion was identified on many of the matte tin finished leads in areas where they were not alloyed with solder as seen in Figure 8.

No effect of bias was observed. Extensive whisker formation was observed on soldered assemblies. For the 32-LQFP, bright Sn finished soldered with SnAgCu solder, many leads were found with whiskers growing on the foot area of leads in areas alloyed with the SnAgCu solder; whiskers were observed to have grown through the flux residue as seen in Figure 9. A few long whiskers were observed on 32 LQFP, bright Sn finish assembled with Sn/Ag/Cu solder as seen in Figure 10. Whiskers were also observed on the shoulders of the 32 LQFP, matte tin, soldered with SnAgCu solder as well as in areas alloyed with solder, as seen in Figure 11.

The key results of DOE 4 are: (1) extensive solder wetting, both with SnPb and SnAgCu solders, led to solder coverage to the shoulder or beyond during the assembly, limiting the available area of non-alloyed areas to examine for Sn whisker growth; (2) the bright tin plating used in this experiment was incompatible with reflow; (3) flux residues did not inhibit whisker growth, nor was there any evidence that the promoted it; (4) whiskers grew from areas of the leads that were alloyed with SAC solder and possibly even from the SAC solder itself; (5) corrosion of the non-alloyed matte Sn finishes was noted after just 1500 hours in the 60°C/85% relative humidity environment; and (6) there was no evidence in this study of any effect of electrical bias or current on whisker growth, in agreement with Hilty et al [7].

2.5 DOE 5

The iNEMI Tin Whisker Accelerated Test Group conducted DOE 5 to better understand the relationship between the results of whisker testing as per JESD201 [8] and field life. The motivation for this work was, therefore, to determine whether a quantitative model (explicit empirical mathematical function) could be defined relating the functional dependence of tin whisker formation and/or length to temperature and humidity storage conditions. If such a function could be found, then the results taken at one temperature humidity "accelerated stress" condition, such as that prescribed in JEDEC201, could be used to estimate whether whiskers would form at any other temperature/humidity condition, for example, at typical operating conditions. To do so, a series of questions had to be answered: (1) Is there a threshold time below which whisker growth does not occur? (2) Is this threshold time a function of temperature and humidity? and (3) What form does this functionality take?

Considering the vast array of whisker results in the literature, and in an attempt to insure the highest probability of finding such a relationship, the iNEMI Tin Whisker Accelerated Test Group developed and conducted a large DOE experimental study. The work began in 2005 with exposure of electroplated Sn on Cu test samples to a wide range of test conditions from 30°C to 100°C with the relative humidity (RH) between 10% and 90%. Moreover, because the interest was in developing a model that was applicable to lead frame devices that have been or will be deployed in the field, all sample were from made at commercial platers using their "whisker-resistant" processes and chemistries. It is common for commercial devices to have Sn plating thicknesses in the range of 3μm – 10μm, thus samples with both 3μm and 10μm-thick were used. To examine the effect of supplier, samples from three different plating suppliers were used. Finally, to explore possible effects of board assembly soldering, the components

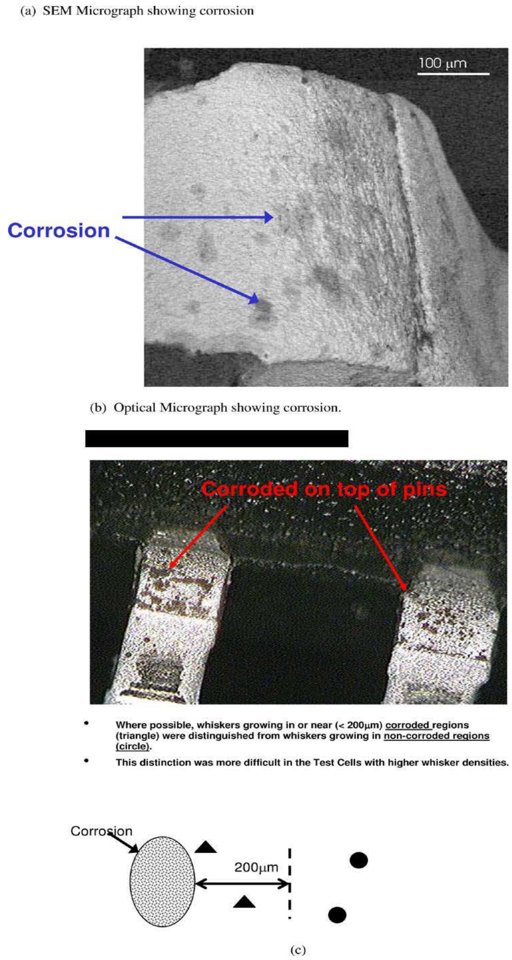


Figure 12. (a) SEM micrograph illustrating the "black spots" indicative of corrosion. (b) Optical micrograph showing corrosion. (c) Schematic illustration of whiskers in regions of corrosion (triangles) and those not in regions of corrosion (circles)

with the 10μm-thick Sn were subjected to a simulated reflow.

This study followed the general procedures given in JESD201 for Sn whisker evaluation. In total DOE 5 consisted of 13 different sample sets, cells, all of which were exposed to 10 different temperature and humidity stress conditions. Storage times ranged from 4000 hours for some storage conditions (85°C/85%RH) to > 3 years for other storage conditions (30°C/10%RH). Further, 96 leads from a total of 6 different packages from each cell in each of the acceleration condition were inspected at each test point. In total the experiment involved inspection of devices over a greater than 3 year period of approximately 500,000 leads on approximately 8200 packaged devices. Because of the size of the experiment and the expectation that other researchers may want to perform an independent analysis of the large data set, Reynolds et al. [13] and Osenbach et al. [15] contain the details of the experimental design, all of the whisker growth and corrosion data, and general observations found in this study.

2.5.1 Corrosion Incubation Time

Corrosion of the Sn platings occurred during long time exposure to high humidity, with examples shown in Figure 12. In this study, the "onset" of corrosion was defined by the initial presence of visible dark spots on the surface of the plating when viewed in an optical microscope or scanning electron microscope (SEM). This time interval was defined as the incubation time for the onset of corrosion of Sn in the absence of an external electric field. In addition to enhancing Sn whisker growth, Sn corrosion, could in and of itself degrade joint reliability. Tin corrosion models were developed as follows: The time interval when corrosion was first observed was defined as the incubation time for the onset of corrosion. The incubation times were used to develop an empirical time–temperature–humidity relationship. Data were broken down into three separate groups: 1) devices that had 3μm-thick non-reflowed platings; 2) devices that had 10μm -thick non-reflowed platings; and 3) devices that had 10μm -thick reflowed platings. The reasons for doing so are detailed in Osenbach and Reynolds. Note as stated in these references, the authors acknowledge the analysis lacks the ability to assign confidence intervals and errors. Furthermore, they acknowledged that other analysis techniques may result in a more complete or different picture and an assessment of error and encourage the reader to do such analysis with the detailed data given in [JESD201].

The grouped data were then fit by Osenbach et al. with each of three commonly used temperature/humidity acceleration functions [12]:

$$\tau_c = A*\exp(-Ea/kT)*\exp[C*(\%RH)] \qquad (1)$$

$$\tau_c = A*\exp(-Ea/kT)*\exp[C/(\%RH)] \qquad (2)$$

$$\tau_c = A*\exp(-Ea/kT)*(\%RH)^{-C} \qquad (3)$$

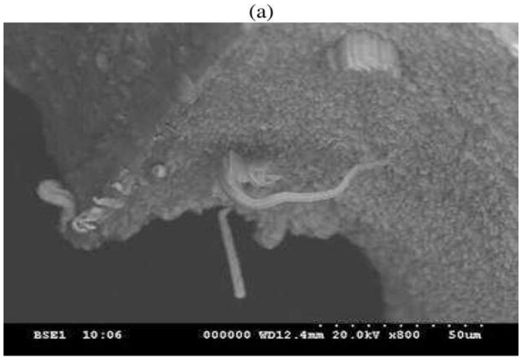
where τ_c is the corrosion incubation time, A is a constant, Ea is the effective activation energy, k is the Boltzmann constant, T is absolute temperature, C is the humidity coefficient, and %RH is the relative humidity in percent. This analysis led to the determination of the fitting parameters A, Ea, and C for the different acceleration functions, Eqns. 1-3. The function that fit the data the best was determined by comparing both the R^2 values determined from the linear regression analysis and by examining the residual error plots for the model prediction versus the actual data. In all cases Eqn. 1 provided the best fitting function, where Table 1 lists the fitting parameters for each group.

Physically, Eqn.1 describes a surface-driven electrochemical limited corrosion process, whereas Eqn. 2 describes a moisture absorption (moisture

Table 1: Fitting parameters for the model:
τ_c= Aexp(Ea/kT)exp(C(RH)

Plating Type	A (hrs)	Ea (eV)	C (1/%RH)	R^2
3µm	0.059	0.38	-0.029	0.91
10µm non-reflowed	0.26	0.33	-0.017	0.74
10µm-reflowed	1.31	0.28	-0.015	0.79
Combined data	0.46	0.31	-0.021	0.72

(a)



(b)

Figure 13. Tin whiskers growing in regions (a) free of corrosion and (b) with corrosion.

adsorption isotherm) limited corrosion process, and Eqn. 3 describes a reaction rate limited corrosion process.[13] Thus, it seems reasonable to conclude that Sn corrosion in a humid environment is in fact electrochemical in nature not moisture absorption and or reaction rate limited.

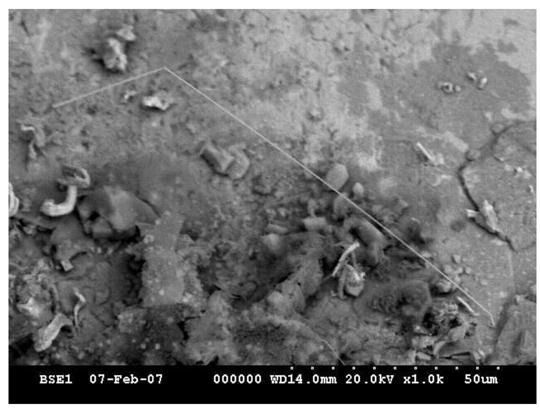
2.3.2 Whisker Incubation Time

Figure 13 a and b show optical micrographs of typical whiskers in corroded and non-corroded regions. Figures 14 and 15 are SEM images of different whisker morphologies observed in this study. Figure 15 illustrates that whiskers, even those in adjacent locations, can show significant variability in diameter. Many whiskers were found with sub-micrometer diameters, while others have diameters in the range of 5 µm to 20 µm.

Table 2 The fitting parameters for the model for incubation time

Plating Type	A (hrs)	Ea (eV)	C (1/%RH)	R^2
3µm	1.15	0.31	-0.031	0.94
10µm non-reflowed	1.16	0.28	-0.017	0.72
10µm-reflowed	0.014	0.41	-0.012	0.90
3µm-corroded	5.16	0.23	-0.018	0.86
10µm non-reflowed-corroded	1.16	0.28	-0.017	0.72
10µm-reflowed-corroded	1.97	0.3	-0.031	0.69
All non-corroded	1.06	0.29	-0.021	0.76
All corroded	1.3	0.28	-0.021	0.66
All	.95	0.29	-0.021	0.70

(a)



(b)

Fig. 14. (a) This SEM photo was taken from a sample in the 100°C/60% RH test cell at the 8000-h inspection interval. This photo shows whiskers with significantly different diameters growing adjacent to each other. (b) This SEM photo shows a long, thin whisker growing in a corroded region among whiskers of different morphologies. (100°C/60%RH test cell at 8000 h).

A similar analysis for developing a time dependent model for the onset of corrosion was used to develop time dependent models for the onset of whisker growth. In this case the devices were grouped into 6 groups: 1) 3µm no corrosion; 2) 10µm no-corrosion; 3) 10µm -reflowed non corrosion; 4) 3 µm corrosion; 5) 10µm corrosion; and 6) 10µm–

Fig. 15. Whisker showing characteristic striations.

reflowed corrosion. In this analysis the onset of whisker formation was defined as the initial observation of a needle-like filament with an aspect ratio (length/width) of $\geq$ 2. Similar to the case for the onset of corrosion, equation (1) was found to provide the best fit to the data for the onset of whisker growth. Table 2 lists the fitting parameters.

In summary, whisker growth was found both in corroded and non-corroded regions of the plating. The incubation time for whisker formation and the onset of corrosion were fit to an exponential function of humidity and an Arrhenius function of temperature for both as-deposited and reflowed tin platings. The effective activation energies and humidity coefficients were found to depend on plating thickness, exposure to reflow, and presence of corrosion. The effective activation energies ranged from 0.23 eV to 0.41 eV and the humidity coefficients ranged from 0.012 to 0.031/(%RH). Corrosion appears to enhance whisker growth. Not discussed here, but an important result discussed in detail in reference 3, the empirically derived mathematical models indicate that 60°C/87% RH appears to be the optimal high-temperature/high-humidity test condition at this time for Sn over Cu substrates. Based on the iNEMI DOE 5, the current JEDEC tests appear to be an efficient predictor of whisker growth behavior of Sn platings.

3. iNEMI TIN WHISKER USERS GROUP

The iNEMI Tin Whisker User Group was involved in the creation of JEDEC JESD22A121 "Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes", was the driver for and a major contributor to JEDEC JESD201A "Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes" and was a major contributor to JEDEC JP002 "Current Tin Whiskers Theory and Mitigation Practices Guideline." [10] The User Group also published a detailed document "iNEMI Recommendations on Lead-Free Finishes for Components Used in High-Reliability Products" [18] (currently at version 4) that is heavily referenced by the industry and is available on the iNEMI web site at the following link: http://thor.inemi.org/webdownload/projects/ese/tin_whiskers/Pb-Free_Finishes_v4.pdf
These documents were driving factors in the industry adoption of tin whisker mitigation practices such as post plating annealing.

4. iNEMI TIN WHISKER FUNDAMENTALS AND MODELING GROUP

The iNEMI Tin Whisker Fundamentals and Modeling Group formed to provide a sustained forum for critical analysis of the underlying driving forces and mechanisms for tin whisker formation. The ultimate goals of the Group were to: (1) determine the underlying mechanisms of whisker formation; (2) identify the material properties of tin deposit, the plating process parameters, and the exposure conditions affecting whisker growth; (3) use the resulting model to predict incubation period, growth rate and maximum length of whiskers based on measurable deposit properties; and (4) use the resulting model to develop an accelerated test and an acceleration factor to determine the potential for future whisker formation.[2]

The iNEMI Tin Whisker Fundamentals and Modeling Group provided theoretical and experimental support for test development within the iNEMI Tin Whisker Accelerated Test Group, as well as to the iNEMI Tin Whisker Users Group in its analyses of potential mitigation strategies in JEDEC standard JESD201. The Group held a series of annual science-based tin whisker workshops in collaboration with NIST, TMS, and ECTC to create a public, international forum for information exchange and debate.[6] The Group chair, G.T. Galyon developed a thorough, annotated bibliography of the tin whisker scientific and engineering literature through 2005 [4]. Results from both the Group's research and research from the Group members' organizations provided significant input for the IPC/JEDEC document JP002, Current Tin Whiskers Theory and Mitigation Practices Guideline, published in March 2006. [See for example, 5, 12, 19-23.]

5. iNEMI ANALYTICAL TIN WHISKER TEST METHOD GROUP

In 2007, these three iNEMI Tin Whisker Groups completed their projects and the teams combined to conduct a major experimental study to develop physics-based whisker formation tests using theories and factors identified by the three previous projects. In forming this Group, the iNEMI members recognized that, although, the test methodology defined in two JEDEC standards (JESD22A121A and

JESD201A) provides a common platform for the industry to assess the whisker growth propensity of Pb-free products, the tests are time and labor-intensive and they do not provide information on the underlying material characteristic that determine the differences in whisker growth performance. For system manufacturers, passing these tests does not necessarily guarantee electronic assemblies to be whisker risk-free, and for component manufactures, these tests do not offer directions for process or material improvements. Therefore the Group determined that further work was needed to investigate and identify the key material properties that drive whisker growth and thus provide better assessment of long term performance of tin whisker growth risk. Key features of the experimental plan include measuring film stress, microstructure evolution on a local, grain scale level through electronic back-scattered diffraction (EBSD) and on a global scale through x-ray texture analysis, and defect formation characteristics as a function of electrolyte, substrate, and subsequent storage conditions. The final report of the iNEMI Analytical Tin Whisker Test Method Group is scheduled to be released in December 2010.

6. CONCLUSIONS

To prepare for the transition to Pb-free surface finishes, iNEMI formed four Tin Whisker Project Groups to deal with short term and long term issues important to the electronics industry worldwide. Through extensive collaborative research and critical analysis, the iNEMI Groups contributed significantly to the development of the test method document JEDEC JESD22A121 and the acceptance requirement document JEDEC JESD201A, as well as the IPC/JEDEC document JP002, Current Tin Whiskers Theory and Mitigation Practices Guideline. Since the development of these industry standards and guidelines, the iNEMI Groups have provided input into their revision as well as made progress in the fundamental understanding of surface finishes properties and environmental conditions that contribute to tin whisker formation. The extensive multi-factorial analyses have helped demonstrate the importance of main effects and the multiple interactions between variables that make the study of tin whiskers such a difficult problem and make the elimination of tin whiskers so difficulty in practice.

6. ACKNOWLEDGEMENTS

The significant contributions of the many members of the four iNEMI Tin Whisker Groups as well as Dr. Robert Pfahl and Dr. Ron Gedney of iNEMI are gratefully acknowledged.

7. REFERENCES

1. Arnold, S. M., “Repressing the Growth of Tin Whiskers,” Proc. IEEE Electronic Component Technology Conference, 75-82, 1959.

2. Boguslavsky, I., “Whiskers: Truth and Mystery, presentation at IPC/NEMI Symposium on Lead-Free Electronics, September 19, 2002, Montreal.

3. Dittes, M., Obemdorff, P., Petit, L., "Tin Whisker formation - results, test methods and countermeasures," *Electronic Components and Technology Conference, 2003. Proceedings. 53rd* , vol., no., pp. 822- 826, May 27-30, 2003

4. Galyon, G. T., “Annotated Tin Whisker Bibliography and Anthology”, IEEE Trans. Electronics Packaging & Manufacturing, 28, (1) 94-122, 2005.

5. Galyon, G.T., Palmer, L., "An integrated theory of whisker formation: the physical metallurgy of whisker formation and the role of internal stresses," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.28, no.1, pp. 17- 30, Jan. 2005

6. Gedney, R.W., "Foreword Special Section on Tin Whiskers," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.30, no.1, pp.1-1, Jan. 2007

7. Hilty, R.D., Corman, N.E., Herrmann, H., "Electrostatic fields and current-flow impact on whisker growth," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.28, no.1, pp. 75- 84, Jan. 2005

8. JEDEC STANDARD JESD201A *Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes,* July 2008, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, www.jedec.org.

9. JEDEC STANDARD JESD22A121A *Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes,* (Revision of JESD22A121.01, December 2005), 2008, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, www.jedec.org.

10. IPC/JEDEC document JP002, Current Tin Whiskers Theory and Mitigation Practices Guideline, 2006, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, www.jedec.org.

11. Lee, C.-J., Reynolds, H., "Tin Whisker Accelerated Test Project," *Electronic Materials and Packaging, 2006. EMAP 2006. International Conference on*, vol., no., pp.1-21, 11-14 Dec. 2006

12. Osenbach, J.W. “Corrosion-induced degradation of microelectronic devices,” *Semicond. Sci. Technol.*, vol. 11, p. 155, 1996.

13. Osenbach, J.W., Reynolds, H.L., Henshall, G., Parker, R.D., Peng Su, "Tin Whisker Test Development—Temperature and Humidity Effects Part II: Acceleration Model Development," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.33, no.1, pp.16-24, Jan. 2010.

14. Reynolds, H.L., Lee, C.J., and Smetana, J, “Tin Whiskers: Mitigation Strategies and Testing,” Chapter 7, Lead-Free Electronics, edited by E. Bradley, C. Handwerker, J. Bath, R. Parker, and R. Gedney, IEEE, 2007.

15. Reynolds, H.L., Osenbach, J.W., Henshall, G., Parker, R.D., Peng Su, "Tin Whisker Test Development—Temperature and Humidity Effects Part I: Experimental Design, Observations, and Data Collection," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.33, no.1, pp.1-15, Jan. 2010

16. Schroeder, V., Bush, P., Williams, M., Vo, N., Reynolds, H. L., "Tin Whisker Test Method Development," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.29, no.4, pp.231-238, Oct. 2006

17. Shibutani, T., Osterman, M., Pecht, M., "Standards for Tin Whisker Test Methods on Lead-Free Components," *Components and Packaging Technologies, IEEE Transactions on Components and Packaging Technologies*, vol.32, no.1, pp.216-219, March 2009.

18. Smetana, J., Lau, J., McDermott, S., Chiang, D., Chin, V., Mei, Z., Parker, R., Benedetto, E., Henshall, G., Schroeder, V., Galyon, G. T., Gedney, R., Coyle, R., Planinsek, F., Reynolds, H., Love, D., and Hilty, R.D., "iNEMI Recommendations on Lead Free Finishes for Components Used in High-Reliability Products," IPC Printed Circuits Expo, APEX and the Designer Summit, Anaheim, CA, Feb. 8-10, 2006, pp. S04-02-1-S04-02-11.

19. Smetana, J. , "Theory of Tin Whisker Growth: “The End Game”," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.30, no.1, pp.11-22, Jan. 2007

20. Su, P., Lee, C.J., Li, L., Xue, J., Khan, B. Moazeni, R., Hartranft, M., "Practical assessment of tin whisker growth risk due to environmental temperature variations," *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th* , vol., no., pp.736-741, 26-29 May 2009

21. Vo, N., Kwoka, M., Bush, P., "Tin whisker test standardization," *Electronics Packaging Manufacturing, IEEE Transactions on* , vol.28, no.1, pp. 3- 9, Jan. 2005

22. Zhao, J.-H., Su, P., Ding, M. Chopin, S., Ho, P.S., "Microstructure-based stress modeling of tin whisker growth," *Electronic Components and Technology Conference, 2005. Proceedings. 55th* , vol., no., pp. 137- 144 Vol. 1, 31 May-3 June 2005

23. Pedigo, A.E., Handwerker, C.A., Blendell, J.E., "Whiskers, hillocks, and film stress evolution in electroplated Sn and Sn-Cu films," *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th* , vol., no., pp.1498-1504, 27-30 May 2008